MULTIMEDIA UNIVERSITY

STUDENT ID NO

MULTIMEDIA UNIVERSITY

FINAL EXAMINATION

TRIMESTER 2, 2022/2023

DSN5101 – COMPUTER ARCHITECTURE AND ORGANIZATION

(All sections / Groups)

12 JULY 2023
9.00 am - 11.00 am
(2 Hours)

INSTRUCTIONS

1. This Question paper consists of **FIVE pages (including this page)** with **FOUR questions.**

2. Attempt **ALL FOUR** questions. Each question carries **10 marks** and the maximum allotted are **40 marks.**

ALL RELEVANT WORKING MUST BE SHOWN.

QUESTION 1

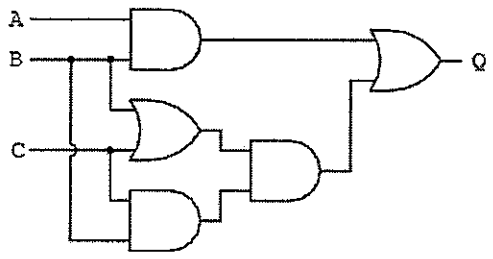

Figure 1

a. Find the Boolean expression for Q and simplify the expression.

(4 marks)

b. Draw the truth table for the simplified expression with SOP standard form.

(4 marks)

c. Draw the logic circuit for the simplified expression.

(2 marks)

QUESTION 2

a. Convert D8.E3 to binary form and then octal form.

(4 marks)

b. Express 5 and negative 3 in
   i) Signed Magnitude form in 4-bits.
   ii) Two's Complement form in 8-bit representation.

(2 marks)

c. Subtract 3 from 5 (i.e: 5 - 3) using two's complement with 8-bit representation.

(4 marks)

Continued...

QUESTION 3

a. Draw and list the inputs for SR, JK, D, and T flip flops and what is the state of the flip flops when all their inputs are 1. (Please label your inputs)

(5 marks)

b. Figure 2 shows a 4-bit shift register circuit configured for right-shift operation, i.e. $D_{in} \rightarrow A$, $A \rightarrow B$, $B \rightarrow C$, $C \rightarrow D$. If the present state of the shift registers ABCD = 1001, show the sequence of values in ABCD for each clock cycle until it reaches the state ABCD =1111.

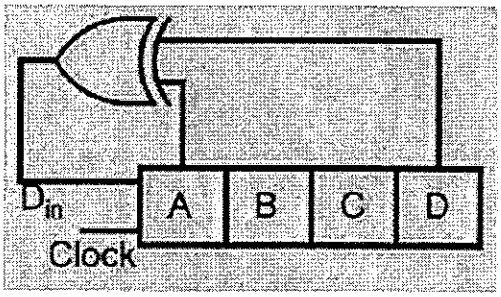

Figure 2

(5 marks)

Continued...

QUESTION 4

a. Explain the differences in instruction set architecture between Intel x86 and ARM.

(2 marks)

b. Name and explain the operation of the three possible techniques for I/O operations.

(2 marks)

c. i) Figure 3 shows an ARM assembly code fragment that performs a certain task. Given the following ARM assembly code, please list out the values in R0 to R5, LR and PC by filling in Table 2. (Add rows if needed)

(3 marks)

```
        MOV     R1, #0x1CC
        MOV     R3, #0x100
        STR     R1, [R1, R3]
        BL      hello
        end
hello   SUB     R1, R1, #0x0c
        STR     R1, [R1, #0x184]
        CMP     R1, #0x184
        BNE     hello
        LDR     R2, [R1, #0x184]!
        MOV     R4, PC
        MOV     R5, LR
        end
```

Figure 3

Register	Contents (in Hex)
R0	
R1	

Table 2

ii) If the first 2 lines of the code was changed to MOV R7, #0x1CC and MOV R5, #0x100, what will happen to R1, R3 and the affected registers?

(2 marks)

End of Page.

Appendix 1

Common ARM Instructions

Instruction	Description
MOV	Move data
MVN	Move and negate
ADD	Addition
SUB	Substraction
MUL	Multiplication
LSL	Logical Shift Left
LSR	Logical Shift Right
ASR	Arithmetic Shift Right
CMP	Compare
CMN	Compare and negate
AND	Bitwise AND
ORR	Bitwise OR
EOR	Bitwise XOR
LDR	Load
STR	Store
LDM	Load Multiple
STM	Store Multiple
B	Branch
BL	Branch with Link
BX	Branch and eXchange
BLX	Branch with Link and eXchange
BIC	Bit Clear
BNE	Branch if not Equal